IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A delay circuit comprising:

a clocked inverter circuit to which a first pulse signal is supplied, said clocked inverter circuit changing the pulse width of said first pulse signal in a first direction; and

a logic circuit to which a second pulse signal output from said clocked inverter circuit and the inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction.

4. (Amended) The delay circuit according to claim 1, wherein said clocked inverter circuit is composed of an NMOS transistor and a PMOS transistor and at least one of a channel width, channel length, threshold voltage, and substrate voltage of the NMOS transistor is different from a channel width, channel length, threshold voltage, and substrate voltage of the PMOS transistor.

5. (Amended) The delay circuit according to claim 4, wherein a ratio of a current driving capability of said PMOS transistor to a current driving capability of said NMOS transistor is set to a value other than one and a rise time of said first pulse signal is made different from a decay time of said first pulse signal.

6. (Amended) A delay circuit comprising:

an inverter circuit controlled by a clock signal to which a first pulse signal is supplied, said inverter circuit changing the pulse width of said first pulse signal in a first direction; and

a logic circuit to which a second pulse signal output from said inverter circuit and the inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction.

Please add the following new claims.

7. (New) The delay circuit according to claim 6, wherein said logic circuit is a NOR circuit and said inverter circuit delays a trailing edge of said third pulse signal.

8. (New) The delay circuit according to claim 6, wherein said logic circuit is a NAND circuit and said inverter circuit delays a leading edge of said third pulse signal.

9. (New) The delay circuit according to claim 6, wherein said inverter circuit is composed of an NMOS transistor and a PMOS transistor, and at least one of a channel width, channel length, threshold voltage and substrate voltage of the NMOS transistor is different from a channel width, channel length, threshold voltage and substrate voltage of the PMOS transistor.

10. (New) The delay circuit according to claim 9, wherein a ratio of a current driving capability of said PMOS transistor to a current driving capability of said NMOS transistor is set at a value other than one and a rise time of said first pulse signal is made different from the decay time of said first pulse signal.

11. (New) A delay circuit applied to a synchronizing circuit comprising:

a first delay line which includes unit delay elements and transfers a forward pulse signal;

a second delay line which includes unit delay elements and transfers a backward pulse signal; and

a state holding section which is brought into a set state or a reset state according to a transfer position of the forward pulse signal transferred along said first delay line and said backward pulse signal transferred along said second delay line in the set state and a clock signal along said second delay line in the reset state,

wherein each of said unit delay elements constituting said first and second delay lines includes:

a clocked inverter circuit to which a first pulse signal corresponding to one of said forward and backward pulse signals output from a preceding delay unit is supplied, said clocked inverter circuit changing a pulse width of said first pulse signal in a first direction; and

a logic circuit to which a second pulse signal output from said clocked inverter circuit and an inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction.

12. (New) The delay circuit according to claim 11, wherein said logic circuit is a NOR circuit and said clocked inverter circuit delays a trailing edge of said first pulse signal.

13. (New) The delay circuit according to claim 11, wherein said logic circuit is a NAND circuit and said clocked inverter circuit delays a leading edge of said first pulse signal.

14. (New) The delay circuit according to claim 11, wherein said clocked inverter circuit is composed of an NMOS transistor and a PMOS transistor, and at least one of a channel width, channel length, threshold voltage and substrate voltage of the NMOS transistor is different from a channel width, channel length, threshold voltage and substrate voltage of the PMOS transistor.

15. (New) The delay circuit according to claim 14, wherein a ratio of a current driving capability of said PMOS transistor to a current driving capability of said NMOS transistor is set at a value other than one and a rise time of said first pulse signal is made different from the decay time of said first pulse signal.